SLRFLR.0009P PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	George A. Zimmerman, et al.	Group Art Unit: 2644
Appl. No.	:	10/603,498	
Filed	:	June 24, 2003	
For	:	METHOD AND APPARATUS FOR PRECODE CROSSTALK MITIGATION	
Examiner	:	Walter F. Briney III	

DECLARATION OF PRIOR INVENTION UNDER 37 C.F.R. § 1.131
BY INVENTOR GEORGE A. ZIMMERMAN

I, George A. Zimmerman, hereby declare as follows,

1. I am a resident of the State of California, U.S.A. I make this declaration on personal knowledge, and if called on sworn as a witness, I could and would competently testify as set forth below.

2. I acknowledge that any willful false statements and the like are punishable by fine or imprisonment, or both under 18 U.S.C. § 1001 and may jeopardize the validity of the application or any patent issuing thereon.

3. All statements made herein are based on my own knowledge, are true, and all statements made on information and belief are believed to be true.

4. Before July 12, 2002, I held the position of Chief Technical Officer with Solarflare Communications.

5. I am a co-inventor of the invention claimed in the above-referenced application (hereinafter Application), which claims priority to U.S. Provisional Patent Application No. 60/424,961 which was filed on November 7, 2002.

6. I am aware that the U.S. Patent and Trademark Office has rejected claims of the application in view of U.S. Patent Application Publication No. US 2004/0022311, serial number 10/195,129 filed on July 12, 2002 (hereinafter Publication)

7. I, as co-inventor, invented the subject matter claimed in the Application before July 12, 2002.

8. I have reviewed the claims as are currently pending.

9. On or before July 12, 2002 I began conceiving the claimed subject matter. In my normal course of research and engineering design, I recorded my inventions in my confidential notebook. I have attached copies of handwritten notes from my notebook in Exhibit A. I have also provided dated printouts from computer simulations, which I reference in and keep with my notebook. These computer simulations are provided in Exhibit B. The content of Exhibit A and Exhibit B has at all times been maintained in secret.

10. Pages are witnessed by Ben Charny, an employee and founder of Solarflare Communications. At all times, as my witness, co-founder, and employee of Solarflare, Ben Charny was under a duty of confidentiality.

11. In reference to the subject matter contained in Exhibit A, Page 11 (shown in upper right hand corner of page) shows a figure wherein a PAM (Pulse Amplitude Modulated) signal is provided to a filter, the output of which is cross-coupled to the other channel. This pre-transmission filtering occurs prior to transmission of the signal through the line. This functions as a precode system and corresponds at least to Figures 10 and 11 of the Application. Directly below the figure shown on Page 11 is a witness signature, dated March, 13, 2001.

12. In reference to the subject matter contained in Exhibit A, Page 18 (shown in upper right hand corner of page) shows a figure wherein a PAM (Pulse Amplitude Modulated) signal is processed to create a cancellation signal, the output of which is cross-coupled to the other channels and combined with the outgoing signal . This pre-transmission processing occurs prior to transmission of the signal through the line. This corresponds at least to Figures 10 and 11 of the Application. Directly below and to the left of the figure shown on Page 8 is a witness signature, dated March 16, 2001.

13. In reference to the subject matter contained in Exhibit B, Page 11 and Page 14 show printouts as used in of computer simulations used to provide theory of operation. These pages are dated April 24, 2001. At all times these pages and the simulations results have been maintained in secret. These print outs show the structure and corresponding method of operation for a system that processes a data signal, prior to transmission, to create cancellation signals, which in turn are provided or combined with the signals on the other channels prior to transmission.

14. On or about January 22, 2002, while employed at Solarflare Communications, I participated in the drafting of a document entitled Theory of Operation. Co-inventor William Jones also contributed to and assisted in the drafting of this document. This document is highly confidential and has not been circulated outside of Solarflare Communications. This document is dated January 22, 2002. A copy of select pages from this document is provided herewith in

Exhibit C. Due to the confidentiality of the Theory of Operation only select pages have been provided.

15. Page 1 of the Theory of Operation as provided in Exhibit C shows that this document is dated before July 12, 2002.

16. The bottom of page 8 and the top of page 9 of Exhibit C discuss use of precode filters and processing in an Ethernet transceiver. The Ethernet environment is understood to utilize more than one channel between transmitters and receiver, usually 4 twisted pair channels or lines per path. This passage shows that W. Jones and myself were in possession of the concept of precode processing in a multi-channel environment before July 12, 2002.

17. Figure 16 on page 15 of Exhibit C illustrates the principle of precode filtering in a multichannel environment. In this figure the signal t1 is processed with element FxP to create a cancellation signal that is provided to a summing junction. The summing junction also receives signal t0. This operation occurs before transmission through the wireline. This passage shows that W. Jones and I were in possession of the concept of precode processing in a multi-channel environment and exchanging cancellation signals from the other transmit signal on the other channels.

18. The text at the top of page 16 of Exhibit C discusses precode processing, namely, adding to the transmit signal, prior to transmission of the transmit signal, 'filtered versions of interfering signals from adjacent channel transmitters.' This passage shows that W. Jones and I were in possession of the concept of precode processing in a multi-channel environment to create a cancellation signal and then combining the cancellation signal, with another outgoing signal, on an adjacent channel. This was done to cancel interference. This occurred prior to transmission of an outgoing signal.

19. As part of the patent application (provisional and utility) filing process, Solarflare Communication hired Chad W. Miller (Weide & Miller, Ltd), attorney of record for the Application, to prepare and file one or more patent applications directed to this invention.

20. Part of my duties at Solarflare Communications is to review invoices sent by Chad W. Miller for accuracy.

21. On or about April 24, 2002 we met with Chad W. Miller to provide an invention disclosure. As part of this invention disclosure, we disclosed the claimed subject matter of the Application to Chad W. Miller. Based on the information provided during this invention disclosure meeting, Chad W. Miller drafted the provisional patent application (60/424,961), to which this application claims priority.

22. Attached as Exhibit D is a copy of the letter and invoice sent from Weide & Miller, Ltd. to Solarflare Communications for the services provided during April and May of 2002. The client

code for reference number, SLRFLR.0004P, which is the Weide & Miller, Ltd. reference number for U.S. provisional application (60/424,961) to which this application claims priority.

23. The invoice entry for SLRFLR.0004P, which is the Weide & Miller, Ltd. reference number for U.S. provisional application (60/424,961), shows that the disclosure was provided on or about April 24, 2002. During this disclosure meeting on April 24, 2002 and during follow-up telephone calls prior to July 12, 2002 both W. Jones and I provided the disclosure of the claimed subject matter to Chad W. Miller.

24. I declare under Penalty of Perjury under the laws of the United States of America that the forgoing is true and correct.

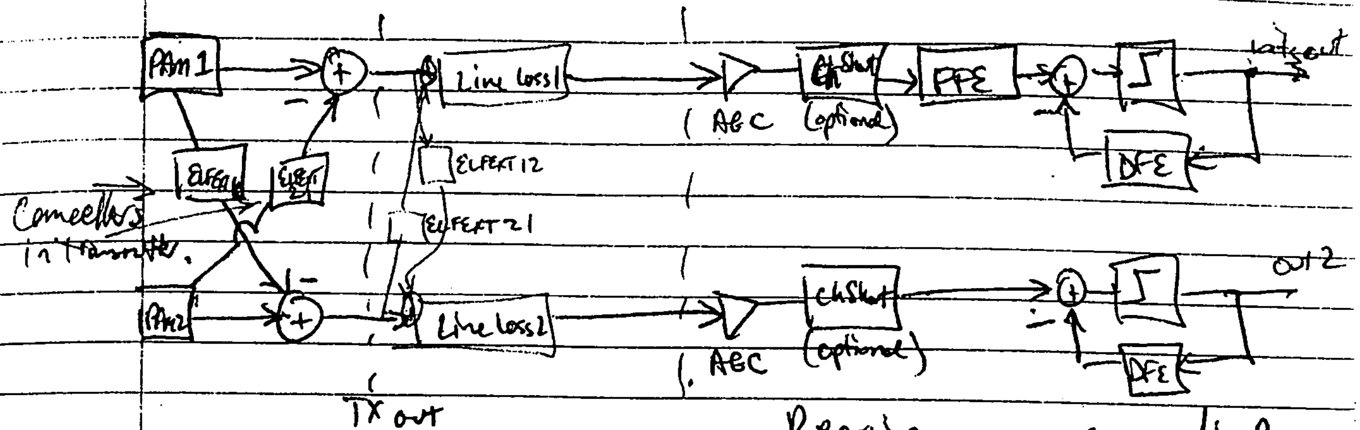
Executed this 31st day of August, 2005.

By: ______________________
George A. Zimmerman

3/13/01

Precoding FEXT Canceller.
pamprec1.svu tested.

Move ELFEXT canceller to transmitter.



Tested in pamprec1.svu, 2 channels. 3/13/01.
3/13/01 witnessed by: 3.13.01

Max peak enhancement $= \sum_{i=0}^{N} |c_i|$ of ELFEXT filter

for 7 tap, this is: 0.5252.

Old pam $= \pm 1$, New $= \pm 1.525$ w/ ± 1 inputs.
~~PAR enhancement will decrease w/ multilevel PAM.~~

Most PAR enhancement is in 1^{st} 2 taps.
(.4366)

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Additional loss in Linear Rcvr based
~~FEXT~~ cancellation due to Noise leakage
through filter
$\rightarrow 10\log_{10}\left(1+\sum_{i=0}^{N} C_i^2\right)$ dB ≈ 0.4 dB for min Φ model

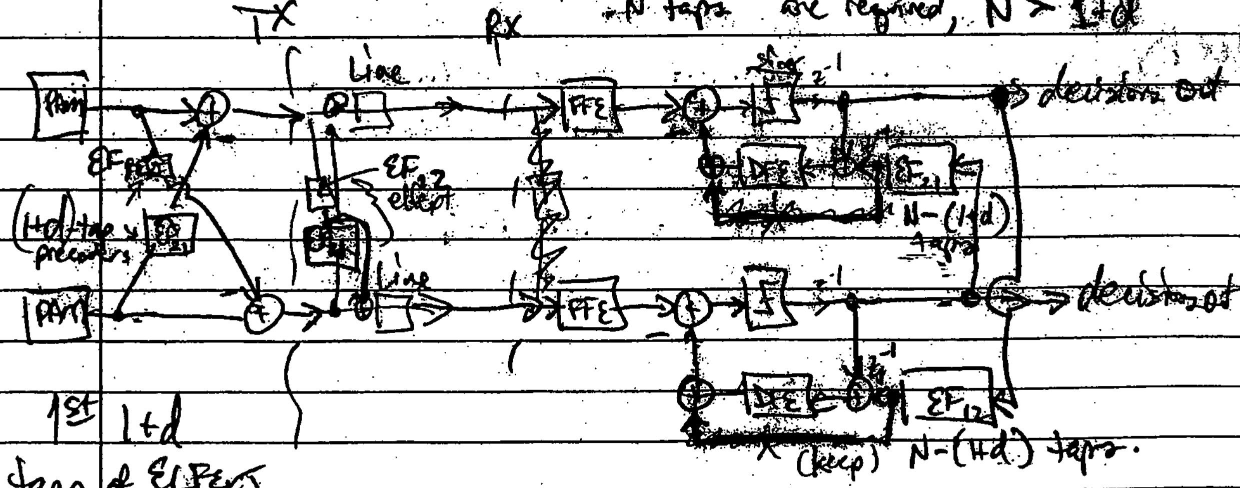
equals precoding TX power loss!

1e6 samples, Abstract expected
Check: Noise = −66.5dB − 4dB − .4 dB = −67.9dB ? (Expected ~ 1.3e-4 pg 25)

So if PAR can be tolerated, do ELFEXT precoding, or, if delay allows, do dec. direct

− Better yet, Hybrid Structure.

FEXT is d samples ahead of signal, + N taps are required, N > 1+d



1st 1+d taps of ELFEXT here

Remaining taps here!

hybrid structure avoids noise problem + delay problems.

3/16/01
witnessed:
3.16.01

for min Φ channel, d = 0, 1 tap at TX, remaining 6 at RX.

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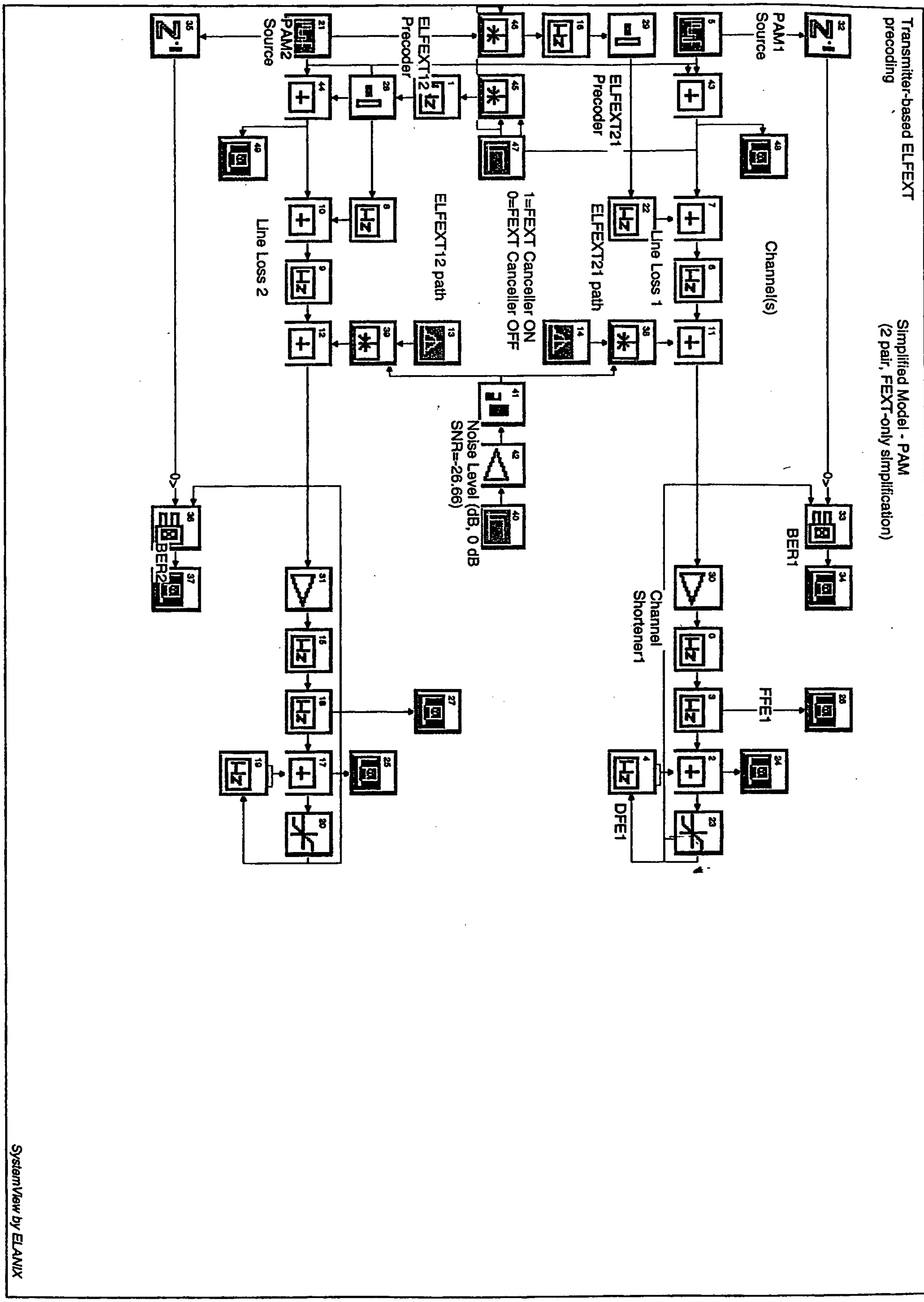
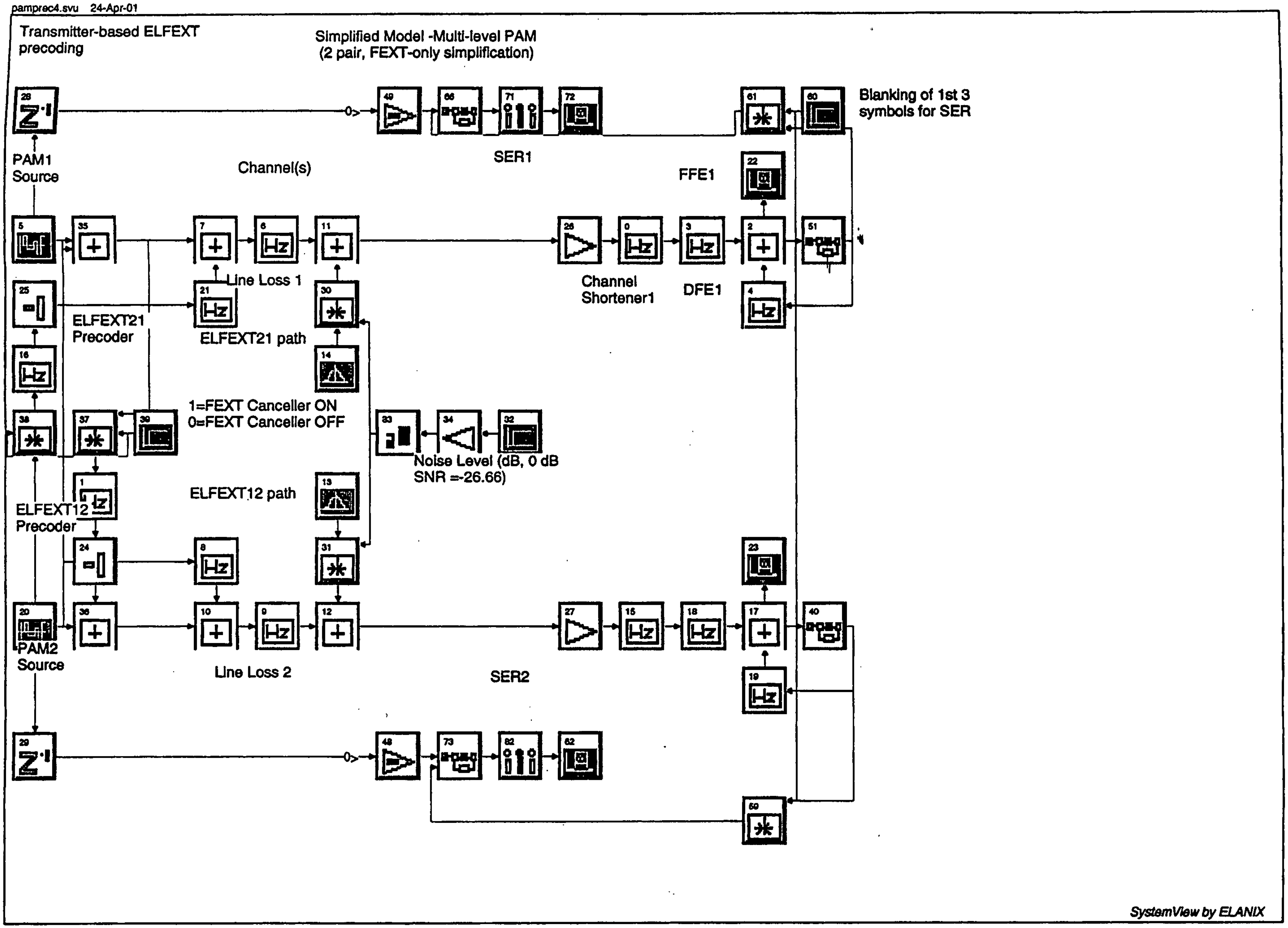
Notebook pg 11



Ref. pg 14


pamprec4.svu 24-Apr-01
Transmitter-based ELFEXT precoding
Simplified Model -Multi-level PAM (2 pair, FEXT-only simplification)
PAM1 Source
Channel(s)
SER1
FFE1
Blanking of 1st 3 symbols for SER
Line Loss 1
ELFEXT21 Precoder
ELFEXT21 path
Channel Shortener1
DFE1
1=FEXT Canceller ON
0=FEXT Canceller OFF
Noise Level (dB, 0 dB SNR =-26.66)
ELFEXT12 path
ELFEXT12 Precoder
PAM2 Source
Line Loss 2
SER2
SystemView by ELANIX

SOLARFLARE
COMMUNICATIONS

Theory of Operation

Revision 0.4

TOD-10100-04

January 22, 2002

frequency interleaving

2.2 Line Codes

pam levels versus capacity versus bandwidth

2.3 Channel Equalization

Because of the severe bandlimiting produced by the wireline channel, channel equalization is necessary to estimate and remove inter-symbol interference (ISI). The equalizer consists of three adaptive filter stages: a partial transmit precoder filter, and feed-forward equalizer (FFE) filter, and a decision feedback equalizer (DFE) filter. A block diagram of the channel equalizer is given in Figure 10. Via the least mean squares (LMS) adaptation algorithm, the equalizer is trained to approximate the condition:

$$H_{txp} \cdot H_{chan} \cdot \frac{H_{ffe}}{1 + H_{dfe}} = 1 \rightarrow \frac{H_{txp} \cdot H_{ffe}}{1 + H_{dfe}} = H_{chan}^{-1}.$$

Because the channel response H_{chan} and the ISI it produces are known only at the receiver, adaptive equalizers are most easily implemented as receive filters. A receive feed-forward equalizer (FFE) can effectively mitigate precursor (future symbol) and postcursor (past symbol) ISI. The FFE uses receive samples to estimate and remove ISI prior to making symbol decisions. However, since an FFE output symbol is the sum of N noisy input symbols, where N is the number of FFE filter taps, the noise per symbol at the FFE output exceeds the noise per symbol at the FFE input. Because of this noise multiplication effect, receive equalizers are typically divided into feed-forward and decision feedback sections. A DFE uses receive symbol decisions to estimate and remove the ISI produced by previous transmit symbols. Since the inputs the decision feedback equalizer (DFE) are sliced receive symbol decisions, not noisy receive samples, the problem of noise multiplication is avoided. The disadvantage of the DFE is that incorrect symbol decisions are fed back to the slicer input causing the potential for symbol error propagation in receivers that operate with minimal receive signal-to-noise ratio. The optimal equalizer architecture depends on the tolerance of the system to FFE noise multiplication and DFE error propagation.

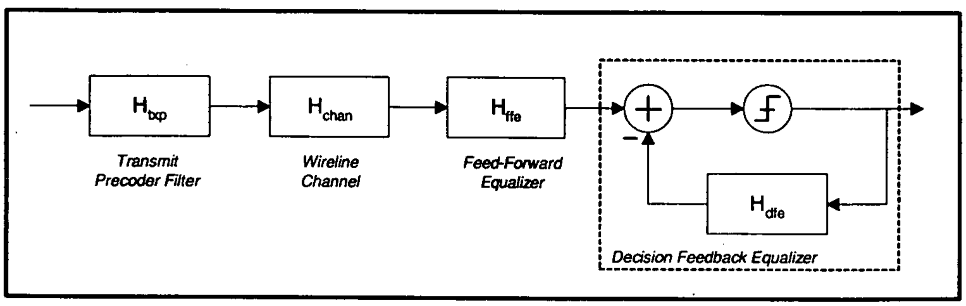


Figure 10: Channel Equalizer Block Diagram

To overcome the noise multiplication and error propagation problems associated with adaptive receive equalizers, transmit precoder filters (Tomlinson-Harishima, dynamics-limited, etc.) can be employed. Like the FFE, transmit precoding can effectively reduce both precursor and postcursor ISI. Unlike the FFE or DFE, the inputs to the transmit precoder filter are noise-free and error-free transmit symbols. Therefore, noise multiplication and error propagation are not a concern. However, adapting the transmit precoder to an unknown channel can be difficult, and the precoder approach has the additional disadvantage that the filtered transmit signal typically has larger peak-to-peak voltage swings than the unfiltered transmit signal, increasing the peak-to-average ratio (PAR) of the transmitter output.

The 10 Gigabit Ethernet transceiver employs an optimal combination of partial transmit precoding and receive adaptive filtering to provide sufficient ISI reduction and minimize the effects of increased PAR, noise multiplication, and error propagation.

2.3.1 Partial Precoding by Spectral Factorization

In the 10 Gigabit Ethernet transceiver, the channel equalizer function is split optimally between a partial transmit pecoder, an FFE, and a tail canceller DFE. The FFE is used to eliminate precursor (future symbol) ISI and the DFE is used to cancel the tail portion of postcursor (past symbol) ISI, defined as ISI produced by all but the first four postcursors. Non-tail ISI, produced by the first four postcursors, is removed by a short transmit precoder filter. This scheme eliminates the first four taps of the DFE (i.e., the first four DFE coefficients equal zero), which typically have the largest filter coefficients, and therefore, contribute most to error propagation. Restricting precoding to the first few postcursors keeps the transmit precoder filter as short as possible, minimizing the increase in PAR caused by filtering the transmit symbols. Via this partial precoding scheme, the effects of transmit precoding on PAR and the effects of DFE symbol error propagation are jointly minimized. Precoding the first four postcursors, instead of using a DFE, has another advantage in that it eases electrical timing constraints associated with implementing feedback filter structures in integrated circuits (i.e., logical race conditions).

Spectral factorization of the FFE filter is used to determine the coefficients of the transmit precoder filter. The FFE is initially trained to cancel precursor ISI and the ISI produced by the first four postcursors. The discrete-time transfer function of the initial FFE filter can be represented as an Nth-order polynomial in z, or by factoring, as the product of N linear terms:

$$H'_{FFE}(z) = \sum_{n=0}^{N} c_n z^{-n}, \qquad (equation\ 1)$$

$$= \prod_{n=1}^{N} (1 - r_n z^{-1}), \qquad (equation\ 2)$$

where c_n are the FFE filter coefficients (i.e., tap weights) and r_n are the roots of the FFE filter polynomial given by $c_0 + c_1 z^{-1} + c_2 z^{-2} + \cdots + c_N z^{-N}$.

The roots of equation 2 above are separated into minimum phase roots (i.e. roots inside the unit circle) and maximum phase roots (i.e., roots outside the unit circle). After training, the terms corresponding to the minimum phase roots determine the transmit precoder filter coefficients and the terms corresponding to the maximum phase roots determine final FFE coefficients:

$$H'_{FFE}(z) = \prod_{n\ \min phase} (1 - r_n z^{-1}) \cdot \prod_{n\ \max phase} (1 - r_n z^{-1})$$

$$= H_{txp} \cdot H_{FFE}$$

2.3.2 Parallel (Multirate) FIR Structures

Because of the time interleaved operation of the transceiver, the equalizer and other time-domain adaptive filters are most efficiently implemented as parallel (multirate) structures. An FIR filter performs a discrete-time convolution of two sequences:

$$y(n) = x(n) * h(n) \leftrightarrow Y(z) = X(z) \cdot H(z) = X \cdot H$$

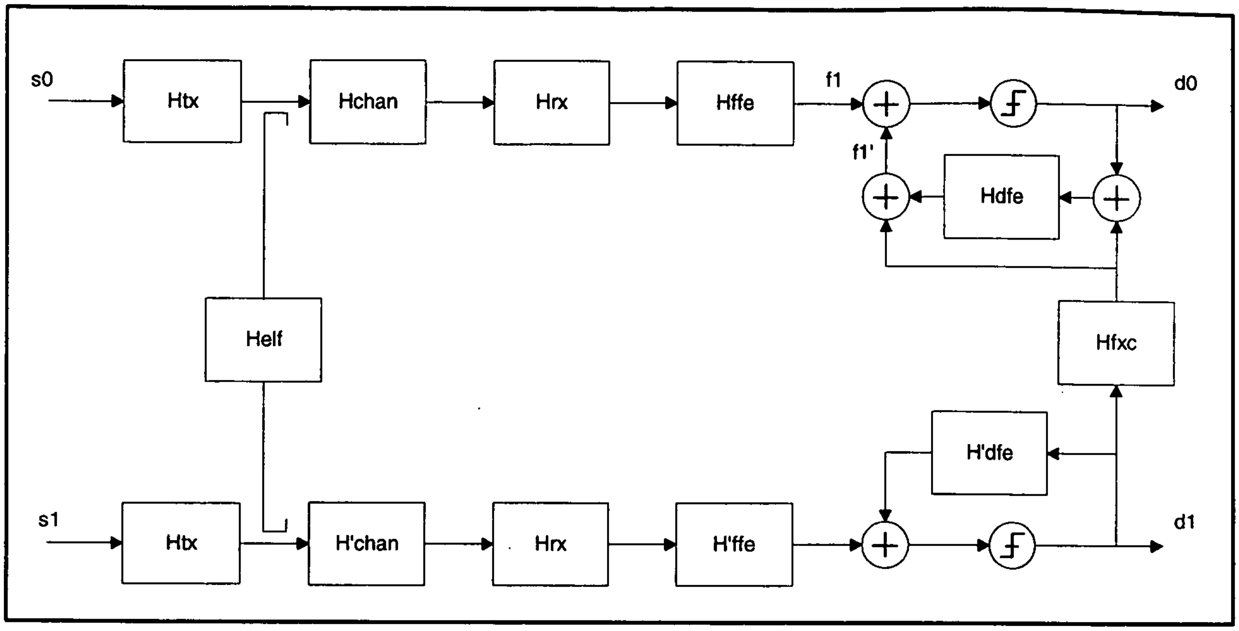


Figure 15: Signal Diagram for Alternative FEXT Canceller Based on ELFEXT Model

A block diagram for the complete fext canceller is shown in Figure 16. As the block diagram shows, the fext canceller filter is split between a precoder portion (FxP) and a canceller portion (FxC). The precoder filter (FxP) at the transmitter eliminates precursor fext that cannot be cancelled at the receiver due to the non-causal nature of the interference. In addition to the fext precoder, the complete fext canceller consists of an elfext FIR filter (FxC) and a fext channel filter formed by the DFE portion of adjacent receivers.

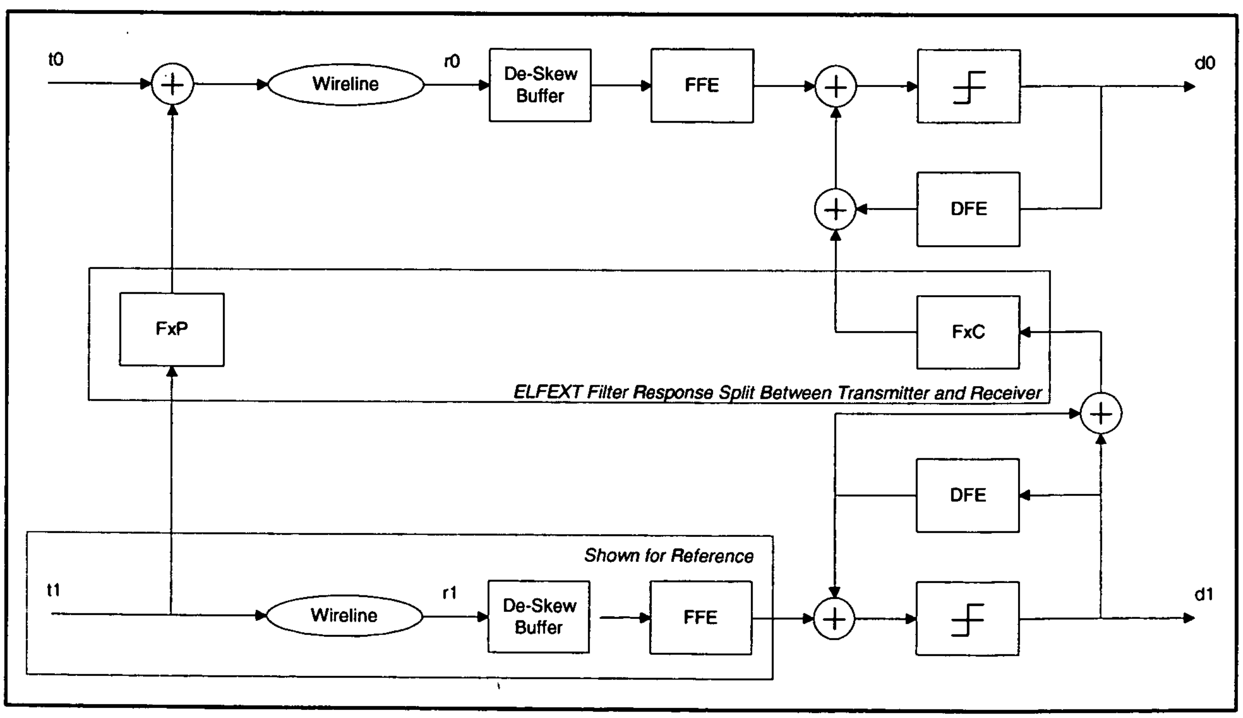


Figure 16: Fext Canceller Block Diagram

The fext precoder eliminates precursor fext by adding, to the transmit signal, filtered versions of interfering signals from adjacent channel transmitters. This intentionally added interference cancels the fext precursor interference coupled across the wireline channel. The interference added at the transmitter by the fext precoder increases the peak excursions of the transmit signal, thereby increasing the peak to average signal ratio (PAR) of the transmit signal. This increases the dynamic range requirements, and therefore the complexity, of the analog front-end (AFE) circuitry.

To minimize the dynamic range impact on the AFE, it is necessary to reduce the length of the precoder filter. Precursor fext is caused by channel group delay and propagation delay skew between adjacent channels. As shown in Figure 17, the propagation delay skew between adjacent channels spans many symbols, and therefore, precursors fext caused by channel skew can be significant. If the propagation delay skew between two adjacent channels is such that the fext at the victim receiver arrives long before the corresponding signal at the target receiver, then it is necessary to precoder the entire elfext response. At the other extreme, if the propagation delay skew between two adjacent channels is such that the fext at the victim receiver arrives long after the corresponding signal at the target receiver, then no precoding is necessary. Removing the propagation delay skew between channels, using de-skewing buffers, equalizes the effects of precursor fext across channels and minimizes the worst case PAR increase at the AFE.

The relationship between propagation delay skew and precursor fext, before and after de-skewing, is shown in Figure 18.

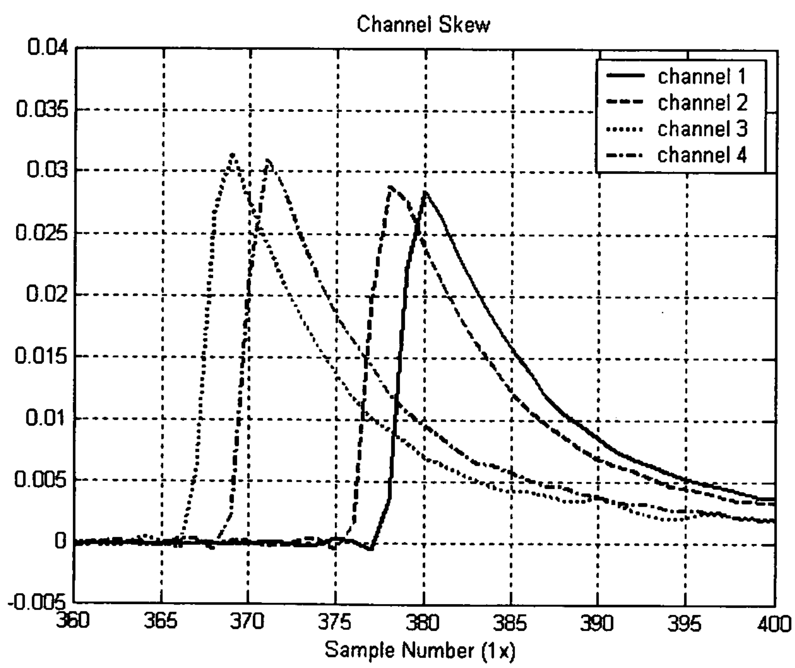


Figure 17: Propagation Delay Skew Between Adjacent Wireline Channels

Three pairs of simulation curves are shown compared to the theoretical curves. Each pair contain represents the partial precoding with DFE operting normally (making feedback errors) and also with a perfect feedback DFE in order to compare the loss due to error propogation. The difference between the pairs is negligible showing that partial precoding has eliminated the error propogation issue. The three pairs show the DFE alone, the DFE followed by a non-interleave (1-way) Viterbi, and the DFE followed by a 4-way interleaved Viterbi. The performance of the 4-way interleaved viterbi approaches the theoretical trellis decoder at higher SNR's, achieving ~3.5 dB of coding gain over the theoretical PAM8 curve at 1E-10 error rate.

WEIDE & MILLER, Ltd.

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330 South 3rd Street
Las Vegas, NV 89101
Telephone (702)-382-4804
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On the web: www.WeideMiller.com

CHAD W. MILLER
REGISTERED PATENT ATTORNEY
LICENSED IN CALIFORNIA & NEVADA

PATENT, TRADEMARK, COPYRIGHT & TRADE SECRET MATTERS

June 7, 2002

Mr. Ben Charny
Executive Vice President and CFO
SolarFlare Communications
9501 Jeronimo Road, Suite 100
Irvine, CA 92618

RE: May and June 2002 Invoice
Our Reference No.: SLRFLR.0001G

Dear Ben:

Enclosed is the invoice for April 01 through May 31, 2002 for services rendered on behalf of SolarFlare Communications.

If you have any questions, please call.

Best Regards,

C. Miller

Chad W. Miller

Weide & Miller, Ltd.
330 South 3rd Street
Suite 1130
Las Vegas, NV 89101
Voice: 702-382-4804
Facsimile: 702-382-4805

Date Generated/Mailed: June 07, 2002

Invoice submitted to: SolarFlare Communications
9501 Jeronimo Road, Suite 100
Irvine CA 92618
Attn: Ben Charny, Executive Vice President & CFO

In Reference To: **Weide & Miller Ref. No.:** SLRFLR.0001G
Subject Matter: General Intellectual Property Representation

Professional Services

			Hrs/Rate	Amount
4/15/02	CWM	Conferences with G. Zimmerman to discuss invention disclosure	0.30 220.00/hr	NO CHARGE
5/8/02	CWM	Prepare status report	0.10 220.00/hr	22.00
		For professional services rendered	0.40	**$22.00**
		Balance due		**$22.00**

SolarFlare Communications

In Reference To:	**Weide & Miller Ref. No.:** SLRFLR.0002P **Subject Matter:** Patent Prosecution **Title:** Transmission Line Equalization **Serial No.:** Not yet assigned

Professional Services

Date		Description	Hrs/Rate	Amount
4/4/02	CWM	Review and revise patent application	4.80 220.00/hr	1,056.00
4/9/02	CWM	Make final changes to draft application; draft e-mail enclosing first draft of patent application to W. Jones; make final changes to draft application	0.40 220.00/hr	88.00
4/24/02	CWM	Conference with B. Jones regarding status of case	0.10 220.00/hr	22.00
		For professional services rendered	5.30	**$1,166.00**
		Previous balance		**$4,708.00**
5/5/02		Payment - thank you. Check No. 1450		($4,708.00)
		Total payments and adjustments		**($4,708.00)**
		Balance due		**$1,166.00**

SolarFlare Communications

In Reference To: **Weide & Miller Ref. No.:** SLRFLR.0003P
Subject Matter: Patent Prosecution
Title: Communication System
Serial No.: Not yet assigned

Professional Services

			Hrs/Rate	Amount
4/10/02	CWM	Create figures and review disclosure material	0.80 220.00/hr	176.00
4/11/02	CWM	Create figures and draft background section	5.60 220.00/hr	1,232.00
4/12/02	CWM	Draft patent application; telephone conference with B. McClellan	5.40 220.00/hr	1,188.00
4/15/02	CWM	Review tape of invention disclosure meeting obtain additional details and gain understanding of method of operation for flow diagrams; take notes regarding same	3.80 220.00/hr	836.00
4/16/02	CWM	Draft patent application and revise figure 7	2.80 220.00/hr	616.00
4/24/02	CWM	Conference with B. McClellan regarding status of case and interleaving of conductors	0.20 220.00/hr	44.00
5/3/02	CWM	Review and revise patent application	2.10 220.00/hr	462.00
5/7/02	CWM	Draft patent application claims	4.20 220.00/hr	924.00
5/8/02	CWM	Continue drafting patent application claims	2.40 220.00/hr	528.00
5/9/02	CWM	Review and revise patent application	1.80 220.00/hr	396.00
5/13/02	CWM	Review and revise patent application and figures; brief conference with inventor	2.70 220.00/hr	594.00
5/29/02	CWM	Review inventor comments and make revisions	4.30 220.00/hr	946.00
		For professional services rendered	36.10	**$7,942.00**
		Previous balance		**$726.00**

		Amount
5/5/02	Payment - thank you. Check No. 1450	($726.00)
	Total payments and adjustments	**($726.00)**
	Balance due	**$7,942.00**

In Reference To: **Weide & Miller Ref. No.:** SLRFLR.0004P
Subject Matter: Patent Prosecution
Title: Method and Apparatus for Joint Equalization and Crosstalk Mitigation
Serial No.: Not yet assigned

Professional Services

			Hrs/Rate	Amount
4/24/02	CWM	Conference with G. Zimmerman regarding upcoming disclosures and disclosure for present case; prepare for meeting by reviewing portion of Theory of Operations document	3.10 220.00/hr	682.00
		For professional services rendered	3.10	**$682.00**
		Balance due		**$682.00**

In Reference To: **Weide & Miller Ref. No.:** SLRFLR.0005P
Subject Matter: Patent Prosecution
Title: Method and Apparatus for Constellation Shaping
Serial No.: Not yet assigned

Professional Services

			Hrs/Rate	Amount
5/6/02	CWM	Review and revise portion of application; create figures and draft portions dealing with constellation shaping	4.20 220.00/hr	924.00
5/12/02	CWM	Review and revise patent application and figures	3.10 220.00/hr	682.00
5/15/02	CWM	Perform final revisions to application; send same with e-mail detailing review instructions; review and respond to two e-mails from B. McClellan during his review process.	0.80 220.00/hr	176.00
5/30/02	CWM	Draft portion of application dealing with constellation mapping	2.80 220.00/hr	616.00
5/31/02	CWM	Review and revise application	0.30 220.00/hr	66.00
		For professional services rendered	11.20	**$2,464.00**
		Balance due		**$2,464.00**